

POWER MOSFET IN SILICON CARBIDE

RELATED APPLICATIONS

This invention is related to copending U.S. patent application Ser. No. 07/893,642 filed on Jun. 5, 1992.

1. Field of the Invention

This invention was made at least partially with government support under the National Aeronautical and Space Administration ("NASA"), Contract Number NAS-25956. The government may have certain rights in this invention. This invention relates to power metal oxide semiconductor field effect transistors ("MOSFETs"), and more particularly to a MOSFET formed in silicon carbide.

2. Background of the Invention

Power semiconductor devices, such as high-power bipolar junction transistors ("HPBT"), power metal oxide semiconductor field effect transistors ("MOSFET"), or gate turn-off thyristors ("GTO"), are semiconductor devices that are capable of controlling or passing large amounts of current and blocking high voltages. Power MOSFETs are generally known and one of the most critical parameters for a power MOSFET is the specific on-resistance (i.e., the resistance of the device in the linear region when the device is turned on). The specific on-resistance for a power MOSFET preferably should be as small as possible so as to maximize the source to drain current per unit area for a given source to drain voltage applied to the MOSFET. The lower the specific on-resistance, the lower the voltage drop is for a given current rating.

Conventional power MOSFETs are manufactured in silicon (Si). MOSFETs formed in Si, however, have certain performance limitations inherent in the Si material itself, such as the thickness of the drain-drift region. The largest contributory factor to specific on-resistance is the resistance of the drain-drift region of the MOSFET. The thickness and doping of the drain-drift region limit the on-resistance. As the rated voltage of a MOSFET is increased, typically the drain-drift region thickness is increased and the drain-drift region doping is decreased. Therefore, the resistance of the drain-drift region increases dramatically. Hence, the thickness of the drain-drift region should be minimized for any given rated voltage so as to minimize the specific on-resistance for the device.

These problems with on-resistance have been recognized and several MOSFET structures have been developed in an attempt to solve the on-resistance problems. Examples of such developments may be seen in U.S. Pat. No. 4,952,991 by Kayuma entitled "Vertical Field-Effect Transistor Having A High Breakdown Voltage And A Small On-Resistance"; U.S. Pat. No. 4,959,699 by Lidow, et al. entitled "High Power MOSFET With Low On-Resistance And High Breakdown Voltage"; U.S. Pat. No. 4,608,584 by Mihara entitled "Vertical Type MOS Transistor"; U.S. Pat. No. 4,931,408 by Hshich entitled "Method of Fabricating a Short-Channel Low Voltage DMOS Transistor"; U.S. Pat. No. 4,974,059 by Kinzer entitled "Semiconductor High-Power MOSFET Device"; U.S. Pat. No. 4,642,666 by Lidow et al. entitled "High Power MOSFET With Low On-Resistance And High Breakdown Voltage"; U.S. Pat. No. 4,965,647 by Takahashi entitled "Vertical MOS Field Effect Transistor Having A High Withstand Voltage And A High Switching Speed"; U.S. Pat. No. 4,860,084 by Shibata entitled "Semiconductor Device MOSFET With V-Shaped Drain Contact"; and U.S. Pat. No. 4,697,201 by Mihara entitled "Power MOSFET with Decreased Resistance In The Conducting State". These

prior attempts to solve the problem included various structures of the Si semiconductor material to try to lower the on-resistance. These prior attempts, however, failed to adequately understand the inherent limitations in the Si semiconductor material itself.

Thus, there presently exists no power MOSFET having low on-resistance and a high temperature range for high voltages.

SUMMARY OF THE INVENTION

The present invention therefore provides a power MOSFET having a low on-resistance and a high temperature range for high voltages. By understanding and developing material processing techniques in silicon carbide, a power MOSFET formed in silicon carbide provides improvement in on-resistance and high temperature performance over conventional power MOSFETs formed in Si.

More particularly, the power metal oxide semiconductor field effect transistor (MOSFET) has a drain region, a channel region, and a source region formed of silicon carbide. The drain region has a substrate of silicon carbide of a first conductivity type and a drain-drift region of silicon carbide adjacent the substrate having the same conductivity type. The channel region is adjacent the drain-drift region and has the opposite conductivity type from the drain-drift region. The source region is adjacent the channel region and has the same conductivity type as the drain-drift region. The MOSFET also has a gate region having a gate electrode formed adjacent a first portion of the source region, a first portion of the channel region, and a first portion of the drain region. A source electrode is formed adjacent a second portion of the source region and a second portion of the channel region. A drain electrode is formed on a second portion of the drain region.

DESCRIPTION OF THE DRAWINGS

Some of the features and advantages of the present invention having been stated, others will become apparent as the description proceeds when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic partial cross-sectional view of a vertical MOSFET formed in silicon carbide having a U-shaped gate contact region according to the present invention;

FIG. 2 is a schematic partial cross-sectional view of a vertical MOSFET having a v-shaped gate contact region ("VMOSFET") formed in silicon carbide according to another embodiment of the present invention;

FIG. 3 is a schematic partial cross-sectional view of a VMOSFET formed in silicon carbide according to a further embodiment of the present invention;

FIG. 4 is a schematic partial cross-sectional view of a VMOSFET formed in silicon carbide according to yet another embodiment of the present invention;

FIG. 5 is a plot of the drain current-voltage characteristics of a VMOSFET formed in silicon carbide having an active area of $6.7 \times 10^4 \text{ cm}^2$ at a temperature of 300 K;

FIG. 6 is a plot of the transconductance gate voltage characteristics of a VMOSFET according to the present invention;

FIG. 7 is a schematic partial cross-sectional view of an ungrounded VMOSFET formed in silicon carbide according to yet another embodiment of the present invention;